instruction fetching means that are connected to said bus to fetch instruction groups via said bus from said memory, certain of said instruction groups including at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located [relative to] a predetermined position from a boundary of said instruction groups;

an instruction register for receiving sequential instructions from a first of said instruction groups from said instruction fetching means, said first of said instruction groups including[an operand or at least two sequential instructions or both] said at least one instruction;

instruction decoding means having a means for generating a counter control signal and an operand control signal;

a counter that is connected to receive said counter control signal from said instruction decoding means;

operand selection means that is responsive to said operand control signal from said instruction decoding means;

instruction supplying means, responsive to said counter to select said predetermined position, for supplying, in succession from said instruction register, said [operand or] sequential instructions [of said first of said instruction groups] to said central processing unit;

said instruction supplying means being further responsive to said counter and said operand selection means for selecting and supplying operands from said predetermined position in said instruction groups to said central processing unit;

said instruction decoding means providing said counter control signal and said operand control signal to cause [for configuring] said instruction supplying means to select from said instruction [register an] groups said operand or instruction or both associated with one of said instructions from said first of said instruction groups.

72(Four Times Amended). The microprocessor system of claim 71 wherein said instruction decoding means further includes means, responsive to a SKIP instruction in said instruction register, for configuring said instruction fetching means such that the next instruction group is supplied to the instruction register, and for configuring said instruction supplying means to supply in succession from said

instruction register, said sequential instructions, beginning with the first instruction in said instruction register from said next instruction group, to said central processing unit, and in which said means for generating the counter control signal, also in response to the SKIP instruction, supplies the counter control signal to reset said counter to zero.

74(Four Times Amended). The microprocessor system of claim 71 further comprising:

a loop counter that is connected to receive a decrement control signal from said instruction decoding means, said instruction decoding means further including means, responsive to a MICROLOOP instruction in said instruction register, configured to supply said decrement control signal to said loop counter, said instruction supplying means being configured to supply from said instruction register beginning with the first instruction in said instruction register, from said first of said instruction groups, to said central processing unit, and in which said means for generating the counter control signal, also in response to the MICROLOOP instruction, supplies the counter control signal for resetting said counter to zero.

82(Three Times Amended). The microprocessor system of claim 80 [further comprising a counter connected to said instruction supplying means, said counter providing a count signal indicative of an instruction of said subsequent one of said instruction groups that is to be provided to said central processing unit by said instruction supplying means,] in which said instruction decoding means supplies said counter control signal to reset said counter [being reset] in response to [receipt by said instruction decoding means of said] a branch-type instruction in said sequential instructions within said first of said instruction groups.

86(Amended). The microprocessor system of claim 80 [further comprising a counter connected to said instruction supplying means,] in which said instruction supplying means [including] includes means for gating said sequential instructions within said instruction register to said central processing unit based on signals produced by said counter.

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87(Amended). The microprocessor of claim 71 wherein said instruction supplying means includes:

[a counter connected to said instruction decoding means,]

a decoder connected to an output of said counter, and

a plurality of gates interposed between said instruction register and said central processing unit, said gates being controlled by signals from said decoder.

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91(Three Times Amended). A microprocessor comprising:

a central processing unit;

an instruction register operatively coupled to said central processing unit;

instruction fetching means for providing sequential instructions within instruction groups to said instruction register wherein certain of said instruction groups include [an operand or at least two sequential instructions or both; said operand or sequential instructions including] at least one instruction that, when executed, causes an access to an operand or an instruction or both , said operand or instruction being located [relative to] at a predetermined position from a boundary of said instruction groups;

instruction decoding means having a means for generating a counter control signal and an operand control signal;

a counter that is connected to receive said counter control signal from said instruction decoding means;

operand selection means that is responsive to said operand control signal from said instruction decoding means;

instruction supplying means, responsive to said counter to select said predetermined position, for successively coupling said sequential instructions of said certain of said instruction groups to said central processing unit; [and]

said instruction supplying means being further responsive to said counter and said operand selection means for selecting and supplying operands from said predetermined position in said instruction groups to said central processing unit; and

said instruction decoding means providing said counter control signal and said operand control signal to cause [for configuring] said instruction supplying means to select [operands] from said instruction [register] groups said operand or instruction or both associated with particular ones of said sequential instructions.

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~~92~~(Three Times Amended). The microprocessor of claim ~~91~~ wherein said instruction decoding means, upon receiving a SKIP one of said sequential instructions from a current one of said instruction groups, configures said instruction fetching means to fetch a next one of said instruction groups to said instruction register, supplies the counter control signal to reset said counter to zero and configures said instruction supplying means to supply a first one of said sequential instructions.

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~~94~~(Three Times Amended). The microprocessor of claim ~~91~~ further comprising a loop counter, said instruction decoding means, responsive to a MICROLOOP instruction within said instruction register, providing a decrement signal to said loop counter and providing the counter control signal to reset said counter to zero, and said instruction supplying means being configured to supply from said instruction register said sequential instructions, beginning with the first instruction in said instruction register, from a current one of said instruction groups, to said central processing unit.

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~~97~~(Three Times Amended). In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions [or] and operands from said memory [instruction register] to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or [at least two sequential instructions] an instruction or both, said [operands] operand or [instructions] instruction being located [relative to] at a predetermined position from a boundary of said instruction groups;

decoding said at least one instruction to determine said predetermined position;

locating said predetermined position; and